Application Note

The Communications Edge ™

Active-Bias Constant-Current Source Recommended for WJ HFET devices

An optional active-bias current mirror is recommended for use with the application circuits shown in WJ's FP1189 and FP2189 datasheets. All WJ HFET's require a negative gate voltage with a positive drain voltage. Generally in a laboratory environment, the gate voltage is adjusted until the drain draws the recommended operating current. The gate voltage required can vary slightly from device to device because of device pinchoff variation, while also varying slightly over temperature.

The active-bias circuit, shown in Figure 1, uses dual PNP transistors to provide a constant drain current into the any FET device, while also eliminating the effects of pinchoff variation. This configuration is best suited for applications where the intended output power level of the amplifier is backed off at least 6 dB away from its compression point. With the implementation of the circuit, lower P1dB values may be measured for a Class-AB amplifier, where the device will attempt to source more drain current while the circuit tries to provide a constant drain current. The circuit should be connected directly in line with where the voltage supplies would be normally connected with the amplifier circuit, as shown in Figure 1. Any required matching circuitry remains the same, although it is not shown in the diagram. This recommended active-bias constant-current circuit adds 6 components to the parts count for implementation, but should cost only an extra \$0.144 to realize (\$0.10 for U1, \$0.0029 for R1, R3, R4, R5, \$0.024 for R2, and \$0.0085 for C1).

Temperature compensation is achieved by tracking the voltage variation with the temperature of the emitter-to-base junction of the two PNP transistors. As a 1st order approximation, this is achieved by using matched transistors with approximately the same I_{be} current. Thus the transistor emitter voltage adjusts the HFET gate voltage so that the device draws a constant current, regardless of the temperature. A Rohm dual transistor - UMT1N - is recommended for cost, minimal board space requirements, and to minimize the variation between the two transistors. Minimizing the variability between the base-to-emitter junctions allow more accuracy in setting the current draw.

The value for the resistor components can be determined with KVL circuit theory. R3 is can be determined by:

$$V_3 = R3 * I_1 \quad (1)$$

$$V_{ds} = V_{be2} + V_3 = V_{be2} + R3 * I_1 \quad (2)$$

$$R3 = \frac{(V_{ds} - V_{be2})}{I_1} \quad (3)$$

Using another equation derived from KVL (equation 4) allows for the derivation of R1 using (3):

$$I_1 = \frac{V_{dd} - V_{be1}}{R1 + R3} \quad (4)$$

$$R1 = \frac{(V_{dd} - V_{ds} + V_{be2} - V_{be1})}{I_1} \quad (5)$$

R2 and R5 can be determined with KVL theory. It is assumed that the no gate current passes through the DUT in forming (7). R4 is inserted to limit the gate voltage V_g so that it may not swing positive under any condition. The value for R4 can be arbitrarily set to be **1 kΩ**

$$R2 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_2} \quad (6)$$

$$R5 = \frac{|V_{gg} - V_g|}{I_2} \quad (7)$$

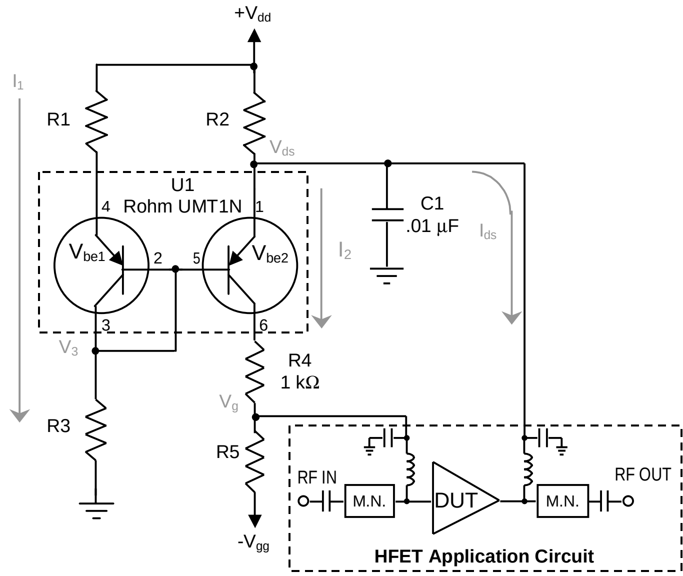

Figure 1. Active-bias schematic

To provide the minimal amount of current variation over temperature, the emitter-to-base junctions of the two transistors should be as closely matched to each other as possible. This can be accomplished by setting the current passing through them I_1 and I_2 to be equal. Thus, V_{be1} and V_{be2} are assumed to be equal. Equations (3), (5), (6), and (7) can be simplified with these assumptions and also setting I_1 and I_2 to be 4 mA. In addition, I_{ds} is assumed to be much larger than I_2 to further simplify the equations.

$$R1 = 250 * (V_{dd} - V_{ds}) \quad (8)$$

$$R2 = (V_{dd} - V_{ds}) / I_{ds} \quad (9)$$

$$R3 = 250 * (V_{ds} - V_{be}) \quad (10)$$

$$R5 = 250 * |V_{gg} - V_g| \quad (11)$$

Using these equations and assuming the V_{be} to be 0.7 V, the following values are recommended for the various WJ HFET devices. The actual calculated values were rounded to realizable standard sizes. A gate voltage V_g of -1 V is assumed to set the required drain current for each of the HFET's.

Parameter	FP1189	FP2189	FP31QF
Pos Supply, V_{dd}	+8 V	+8 V	+9 V
Neg Supply, V_{gg}	-5 V	-5 V	-5 V
Vds	+7.75 V	+7.75 V	+8.75 V
Ids	125 mA	250 mA	450 mA
R1	62 Ω	62 Ω	62 Ω
R2	2.0 Ω	1.0 Ω	0.56 Ω
R3	1.8 kΩ	1.8 kΩ	2 kΩ
R4	1 kΩ	1 kΩ	1 kΩ
R5	1 kΩ	1 kΩ	1 kΩ

Some care should be taken to verify that the power dissipation (I_{ds}^2*R2) through R2 complies with the package size chosen. In addition, the accuracy of I_{ds} is determined directly by the precision of the R2 value. Therefore, a high precision R2 component is recommended. This can also be achieved by increasing the supply voltage V_{dd}. All other resistors can be chosen to be a standard 0603 package size for standard 5% precision tolerance